

SEP 28 2005



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September 28, 2005

To: **Telephone:** **Fax Number:**
Examiner Steven Ho Yin LOKE (571) 272-1657 (571) 273-8300

Commissioner for Patents
Alexandria, VA 22313-1450

From: J. Y. Ikegami **Client-Matter Number:** 2102397-991320 (352003)
Reg No. 51,115
650-833-2104 **New #352003-991320/US**

Re: U.S. Patent Application No. 10/762,156

Pages: - 6 - (including this form) **Originals:** ☐ will be mailed ☒ will not be mailed
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Attorney Docket No. 2102397-991320 (352003)
U.S. Patent Application No. 10/762,156
Filing Date: January 20, 2004
Title: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING AN OBLIQUE GLOBAL SIGNAL WIRING AND SEMICONDUCTOR INTEGRATED CIRCUIT WIRING METHOD

Enclosed is: 1. Response to the Restriction Requirement mailed on August 31, 2005

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Maria Paula Kovacs

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Maria Paula Kovacs

Appl. No. : 10/762,156
Applicant : Kojima et al.
Filed : January 20, 2004
TC/A.U. : 2811
Examiner : Steven Ho Yin Loke

Confirmation No. 4963

Docket No. : 2102487-991320 (352003)
Customer : 26379
No.

Title: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING AN OBLIQUE
GLOBAL SIGNAL WIRING AND SEMICONDUCTOR INTEGRATED
CIRCUIT WIRING METHOD

RESPONSE TO RESTRICTION REQUIREMENT

M/S: AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request the Examiner to consider the following Response in reply to the
Office Action, mailed on August 31, 2005, for the above-referenced application.

Amendments to the Claims are reflected in the listing of claims, which begins on page 2
of this paper.

Remarks/Arguments begin on page 4 of this paper.